49. The method of claim 25, further comprising providing an indication of a status of the sensor output to an external device.

REMARKS

Claims 1-27, 31-40, and 49 are currently pending in the application and all claims stand rejected. Applicants propose herein to amend claims 1 and 37. Applicants respectfully request reconsideration of the amended application in view of the remarks set forth below.

Obviousness Rejections Under 35 U.S.C. § 103

To reject a claim or claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. M.P.E.P. § 2142. When establishing a prima facie case of obviousness, the Examiner must set forth evidence showing that the following three criteria are satisfied:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references (or references when combined) must teach or suggest all the claim limitations.
> M.P.E.P. § 2143.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on the applicant's disclosure. M.P.E.P. § 2142 (citing *In re Vaeck*, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991)). Also, the evidentiary showing of a motivation or suggestion to combine prior art references "must be clear and particular." *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999).

Obviousness Rejection Based on United States Patent 5,675,297 to Gose et al. in View of United States Patent 5,713,030 to Evoy

Claims 1, 9, 17, and 37-40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent 5,675,297 to Gose et al. (hereinafter "Gose") in view of United States Patent 5,713,030 to Evoy (hereinafter "Evoy"). Applicants respectfully traverse this rejection as set forth below.

Claim 1, as amended, recites:

> 1. (Three Times Amended) A thermal management system ***for an integrated circuit die*** comprising:
> a temperature detection element formed ***directly on the integrated circuit die***, the temperature detection element including at least one temperature sensor having an output;
> a power modulation element formed ***directly on the integrated circuit die***, the power modulation element to reduce power consumption of the integrated circuit die in response to the output of the at least one temperature sensor;
> a control element formed ***directly on the integrated circuit die***, the control element including at least one register to provide an enable/disable bit for the thermal management system; and
> a visibility element formed ***directly on the integrated circuit die***, the visibility element to indicate a status of the output of the at least one temperature sensor.

Each of claims 9 and 17 recites similar limitations. Claim 37, as amended, recites:

> 37. (Twice Amended) A method of forming a thermal management system ***for an integrated circuit die*** comprising:
> forming a temperature detection element ***directly on the die***;
> forming a power modulation element ***directly on the die***;
> forming a control element ***directly on the die***; and
> forming a visibility element ***directly on the die***.

The Examiner states that the Gose patent teaches "a thermo management system with power modulation element, control element, [and] visibility element to indicate

status of the output." Final Office Action, at page 3. The Examiner further states "Gose ***does not disclose*** the temperature detection element formed on an microprocessor integrated circuit die." *Id.* To overcome the lack of teaching in Gose, the Examiner relies upon Evoy, stating that "Evoy disclose the computer system with temperature detection element ***formed on an microprocessor integrated circuit die***, with plurality of functions with memory ***(fig. 3)***, to integrated the function of the microprocessor with temperature control with reference voltage ***(fig. 3)***." *Id.* (emphasis added). The Examiner further states:

> Applicant argue that no art teaches 'formed directly on an IC die' while it is obvious to formed the temperature detect unit directly on an IC in order to improve the reliability of the IC chip for an ordinary skill in the art at the time of the invention. Evoy shows an integrated the function of the microprocessor with temperature control with reference voltage ***(Evoy fig. 3)***. Many features including temperature detection functions are pack into IC die, for example memory modules, temperature detection, memory/bus controller among the few that is common to integrate at the time of the invention on an IC design. Final Office Action, at page 7 (emphasis added).

The Gose patent discloses a conditional protection circuit 10 having a pulse-width modulation (PWM) circuit 12, a thermal shutdown circuit 20, and a TSD (thermal shutdown) detection circuit 16. Column 1, Lines 14-27; FIG. 1. The Evoy patent is directed to a thermal management device and method for a microprocessor. Column 1, Lines 5-7.

However, in contrast to the Examiner's assertion that Evoy teaches a "temperature detection element formed on [a] die," Evoy discloses a thermal management system that is provided on a "**separately packaged** integrated circuit clock chip . . . coupled to the processor for controlling the frequency of operation of the processor." Column 3, Lines 14-25; Column 3, Lines 60-67 through Column 4, Lines 1-5; Column 4, Lines 12-23. Note specifically that FIG. 3 of Evoy, which figure the Examiner seems to particularly rely upon, shows a thermister circuit (item 116) disposed on a chip **separate from the processor chip whose thermal characteristics are being monitored**.

Each of claims 1, 9, 17, and 37 is directed to a thermal management system for an integrated circuit die, **wherein all elements of the thermal management system are formed directly on the die itself (i.e., the die whose thermal characteristics are being managed)**. Claims 1 and 37 have each been amended to clarify this point.

It should be further noted that the thermister circuit shown on the separate clock chip in FIG. 3 of Evoy teaches away from the present invention, as the thermal management system of the present claimed invention is located directly on the die whose thermal characteristics are being managed. See M.P.E.P. § 2145(X)(D).

The Examiner also asserts that "[m]any features including temperature detection functions are pack into IC die, for example memory modules, temperature detection, memory/bus controller among the few that is common to integrate at the time of the invention on an IC design." The cited examples of "memory modules" and "memory/bus controller" are inapt, as no claim recites such limitations.

In summary, the Gose and Evoy patents, either individually or in combination, fail to teach or suggest at least the above-noted limitations. Therefore, a prima facie case of obviousness can not be made out with respect to claims 1, 9, 17, and 37 based upon the Gose and/or Evoy patents, respectively, and each of claims 1, 9, 17, and 37 is nonobvious in view of Gose and Evoy.

Also, if an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 38-40 are allowable as depending from nonobvious, independent claim 37.

Obviousness Rejection Based on United States Patent 5,675,297 to Gose et al. in View of United States Patent 5,713,030 to Evoy and Further in View of United States Patent 5,838,578 to Pippin

Claims 2, 6, 7, 8, 10, 14, 15, 16, 18, 22-27, 31-33, 35, and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gose in view of Evoy and further in view of United States Patent 5,838,578 to Pippin (hereinafter "Pippin"). Applicants respectfully traverse this rejection as set forth below.

Claims 2, 6-8, 10, 14-16, 18, and 22-24

The respective disclosures of Gose and Evoy are summarized above. The Pippin patent discloses a programmable thermal sensor implemented in an integrated circuit. Column 2, Lines 7-8. As noted above, the Gose and Evoy patents, either individually or in combination, fail to teach or suggest a thermal management system for an integrated circuit die, wherein all elements of the thermal management system are formed directly on the integrated circuit die, and the Pippin patent also fails to teach or suggest these limitations.

In sum, the Gose, Evoy, and Pippin patents, either individually or in combination, fail to teach or suggest at least the above-noted limitations of each of independent claims 1, 9, and 17. Thus, independent claims 1, 9, and 17, respectively, are nonobvious in view of Gose, Evoy, and Pippin.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 2 and 6-8 are allowable as depending from nonobvious, independent claim 1. Similarly, claims 10 and 14-16 are allowable as depending from nonobvious, independent claim 9, whereas claims 18 and 22-24 are allowable as depending from nonobvious, independent claim 17.

Claims 35 and 36

Claim 34 is directed to an "apparatus" and recites, in part, a "visibility element . . . including a register to indicate the status of the output of the at least one temperature sensor; a register providing a sticky bit; a counter to count a number of lost clock cycles resulting from operation of the apparatus; and circuitry to generate an interrupt when the output of the at least one temperature sensor transitions to a different state."

The respective disclosures of the Gose, Evoy, and Pippin patents are summarized above. None of the Gose, Evoy, and Pippin patents, either individually or in combination, discloses a visibility element that includes all of the recited limitations (i.e., a register to indicate status at output of temperature sensor, a register providing a sticky bit, and a counter to count lost clock cycles), and the Examiner has failed to set forth any specific teaching or suggestion from Gose, Evoy, and/or Pippin to the contrary. Note that

the Examiner expressly states – Final Office Action, at page 6 – that Pippin fails to disclose a sticky bit.

As the Gose, Evoy, and Pippin patents, either individually or in combination, fail to teach or suggest at least the above-noted limitations of claim 34, a prima facie case of obviousness has not been set forth with respect to claim 34. Thus, claim 34 is nonobvious in view of the Gose, Evoy, and Pippin patents.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Thus, claims 35 and 36 are allowable as depending from nonobvious, independent claim 34.

Claims 25-27 and 31-33

Claim 25 recites:

> 25. A method comprising:
> providing an enable bit to a register to activate a thermal management system of a die;
> measuring a temperature on the die with a sensor of the thermal management system;
> providing a first state at an output of the sensor when the temperature is below a trip point;
> providing a second state at the sensor output when the temperature equals or exceeds the trip point;
> in response to the sensor output having the second state, engaging a power reduction mechanism for a specified time period to reduce power consumption of the die;
> polling the sensor output after expiration of the specified time period;
> engaging the power reduction mechanism for at least another one of the specified time periods if the sensor output exhibits the second state; and
> halting the power reduction mechanism when the sensor output exhibits the first state.

It is respectfully pointed out that the Examiner has not set forth any evidence as to the teaching or suggestion in the prior art references of any of the above limitations of

independent claim 25 and, therefore, the Examiner has **failed to set forth a prima facie case of obviousness with respect to claim 25** and its dependent claims (claims 26, 27, and 31-33). Accordingly, with respect to claims 25-27 and 31-33, the **Patent Office has not satisfied it's burden of factually supporting any conclusion of prima facie obviousness**. See M.P.E.P. § 2142.

Obviousness Rejection Based on United States Patent 5,675,297 to Gose et al. in View of United States Patent 5,713,030 to Evoy and Further in View of United States Patents 6,137,329 to Kardash and 6,336,593 to Bhatnagar

Claims 3-5, 11-13, and 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Gose in view of Evoy and further in view of United States Patent 6,137,329 to Kardash (hereinafter "Kardash") and United States Patent 6,336,593 to Bhatnagar (hereinafter "Bhatnagar"). Applicants respectfully traverse this rejection as set forth below.

The respective teachings of Evoy and Gose are summarized above. The Kardash patent discloses a controller for controlling the voltage slew-rate of an inductive load connected to a field effect transistor and a controller for driving an inductive load. Column 2, Lines 14-54. The Bhatnagar patent discloses a multi-point compact electronic control unit having an electronic digital thermostat. Column 2, Lines 59-68 through Column 3, Lines 1-27.

As noted above, the Gose and Evoy patents, either individually or in combination, fail to teach or suggest a thermal management system for an integrated circuit die, wherein all elements of the thermal management system are formed directly on the integrated circuit die. Kardash and Bhatnagar, respectively, also fail to teach or suggest such limitations.

Accordingly, Gose, Evoy, Kardash, and Bhatnagar, either individually or in combination, fail to teach or suggest at least the above-noted limitations of independent claims 1, 9, and 17, respectively. Thus, independent claims 1, 9, and 17 are nonobvious in view of Gose, Evoy, Kardash, and Bhatnagar.

If an independent claim is nonobvious, then any claim depending from the independent claim is also nonobvious. M.P.E.P. § 2143.03 (citing *In re Fine*, 5

U.S.P.Q.2d 1596 (Fed. Cir. 1988)). Therefore, claims 3-5, 11-13, and 19-21 are allowable as depending from nonobvious, independent claims 1, 9, and 17, respectively.

Obviousness Rejection Based on United States Patent 5,838,578 to Pippin in View of United States Patent 6,101,516 to Wolrich et al.

Claims 34 and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pippin in view of United States Patent 6,101,516 to Wolrich et al. (hereinafter "Wolrich"). Applicants respectfully traverse this rejection as set forth below.

Claims 34

Claim 34 recites:

> 34. (Amended) An apparatus comprising:
> a temperature detection element, the temperature detection element including at least one temperature sensor having an output;
> a power modulation element, the power modulation element to reduce power consumption of an integrated circuit die in response to the output of the at least one temperature sensor;
> a visibility element, the visibility element to indicate a status of the output of the at least one temperature sensor, the visibility element including
> a register to indicate the status of the output of the at least one temperature sensor;
> a register providing a sticky bit;
> ***a counter to count a number of lost clock cycles resulting from operation of the apparatus***; and
> circuitry to generate an interrupt when the output.

The Examiner states that the Pippin patent discloses a "counter to count number of clock" cycles. Final Office Action, at page 5. The Applicants respectfully disagree that Pippin discloses the claimed "counter to count a number of lost clock cycles resulting from operation" of the claimed apparatus.

Pippin discloses a programmable thermal sensor implemented in an integrated circuit. Column 2, Lines 7-8. The only counter shown and described in the Pippin patent

is the counter 950 illustrated in FIG. 9. However, as stated in the Pippin patent, the "counter 950 is configured as a frequency divider such that a clock frequency, from the external clock 945, is input" and the "counter 950 generates a new clock frequency based on the counter value." Column 12, Lines 35-40. Thus, according to the express description of the counter 950 provided in the written specification of the Pippin patent, the counter 950 does not count a number of lost clock cycles. The Wolrich patent discloses a method and apparatus for predicting a normalization shift during floating point add-subtract operations – Column 2, Lines 29-67 – and the Wolrich patent also fails to disclose any counter to count a number of lost clock cycles resulting from operation of a thermal management system.

Thus, the Pippin and Wolrich patents, either individually or in combination, fail to teach or suggest at least the above-noted limitations of claim 34. Accordingly, claim 34 is nonobvious in view of the Pippin and Wolrich patents.

Claim 49

Claim 49 depends from claim 25 and includes all the limitations recited therein. The Examiner has not set forth any evidence as to any of the limitations of claim 49 (or claim 25) and, therefore, the Examiner has **failed to set forth a prima facie case of obviousness with respect to claim 49**. Accordingly, with respect to claim 49 (and claim 25), the **Patent Office has not satisfied it's burden of factually supporting any conclusion of prima facie obviousness**. See M.P.E.P. § 2142.

CONCLUSION

Applicants submit that claims 1-27, 31-40, and 49 are in condition for allowance and respectfully request allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 02-2666.

Respectfully submitted,

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Angie C. Farr 12.16.02
Signature *Date*

MARKED UP VERSION OF THE AMENDED CLAIMS

1. (Three Times Amended) A thermal management system [located on] for an integrated circuit die comprising:

a temperature detection element formed directly on [an] the integrated circuit die, the temperature detection element including at least one temperature sensor having an output;

a power modulation element formed directly on the integrated circuit die, the power modulation element to reduce power consumption of the integrated circuit die in response to the output of the at least one temperature sensor;

a control element formed directly on the integrated circuit die, the control element including at least one register to provide an enable/disable bit for the thermal management system; and

a visibility element formed directly on the integrated circuit die, the visibility element to indicate a status of the output of the at least one temperature sensor.

37. (Twice Amended) A method of forming a thermal management system [on] for an integrated circuit die comprising:

forming a temperature detection element directly on [a] the die;

forming a power modulation element directly on the die;

forming a control element directly on the die; and

forming a visibility element directly on the die.